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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/802,774 | 03/18/2004 | Lee D. Genz | 42339-199897 | 4667 |

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| EXAMINER | |
|---|---|
| LEVIN, NAUM B | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2825 | |

DATE MAILED: 04/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/802,774 | GENZ ET AL. | |
| | Examiner | Art Unit | |
| | Naum B. Levin | 2825 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *18 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Specification*

The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

### Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.
(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
(d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT
(e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC (See 37 CFR 1.52(e)(5) and MPEP 608.05. Computer program listings (37 CFR 1.96(c)), "Sequence Listings" (37 CFR 1.821(c)), and tables having more than 50 pages of text are permitted to be submitted on compact discs.) or
REFERENCE TO A "MICROFICHE APPENDIX" (See MPEP § 608.05(a). "Microfiche Appendices" were accepted by the Office until March 1, 2001.)
(f) BACKGROUND OF THE INVENTION.
(1) Field of the Invention.
(2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
(g) BRIEF SUMMARY OF THE INVENTION.
(h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
(i) DETAILED DESCRIPTION OF THE INVENTION.
(j) CLAIM OR CLAIMS (commencing on a separate sheet).
(k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
(l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

**Content of Specification**

(f) Background of the Invention: See MPEP § 608.01(c). The specification should set forth the Background of the Invention in two parts:

(1) Field of the Invention: A statement of the field of art to which the invention pertains. This statement may include a paraphrasing of the applicable U.S. patent classification definitions of the subject matter of the claimed invention. This item may also be titled "Technical Field."

(2) Description of the Related Art including information disclosed under 37 CFR 1.97 and 37 CFR 1.98: A description of the related art known to the applicant and including, if applicable, references to specific related art and problems involved in the prior art which are solved by the applicant's invention. This item may also be titled "Background Art."

1. BRIEF SUMMARY OF THE INVENTION is missed in the specification.

Appropriate corrections are required.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-36 are rejected under 35 U.S.C. 103(a) as being unpatentable by McGaughy in view of Gilbert et al. (US Patent 5,805,861).

3. As to claim 1, 10, 19, and 28 McGaughy teaches:

(1) A machine-accessible medium that provides instructions, which when executed by a computing platform, cause said computing platform to perform operations comprising a method of ([0066]- [0067]):

obtaining a first subcircuit layout design (receiving a SPICE-like source file 510; source file 510 typically includes a plurality of `subcircuit`-defining expressions such as 511 through 514. Each subcircuit descriptor (e.g., 511) explicitly defines for its respective subcircuit, at least one or more externally-exposed nodes (Nx's, each of which, may be alternatively termed as being an external `port`). The Nx's provide an interface by way of which the corresponding subcircuit and its other internal components may interact with yet other described-subcircuits of the to-be-simulated system and/or with the outside world) ([0119]- [0120]);

obtaining a second subcircuit layout design (receiving a SPICE-like source file 510; source file 510 typically includes a plurality of `subcircuit`-defining expressions such as 511 through 514. Each subcircuit descriptor (e.g., 511) explicitly defines for its respective subcircuit, at least one or more externally-exposed nodes (Nx's, each of which, may be alternatively termed as being an external `port`). The Nx's provide an interface by way of which the corresponding subcircuit and its other internal components may interact with yet other described-subcircuits of the to-be-simulated system and/or with the outside world) ([0119]- [0120]);

generating a first topology graph for said first subcircuit layout design (generating from the received source file, a Primitives-containing DataBase (PDB) 520 having: a Topologies-describing DataBase (TDB) 520a, a separated, but element-by-element

tracking, Models/geometries-describing DataBase (F-GDB) 520b, and a separated but further element-by-element tracking, Naming/re-naming DataBase (NDB) 520c) ([0119]);

generating a second topology graph for said second subcircuit layout design (generating from the received source file, a Primitives-containing DataBase (PDB) 520 having: a Topologies-describing DataBase (TDB) 520a, a separated, but element-by-element tracking, Models/geometries-describing DataBase (F-GDB) 520b, and a separated but further element-by-element tracking, Naming/re-naming DataBase (NDB) 520c) ([0119]);

comparing said first topology graph and said second topology graph to obtain a comparison result (A second test 402 (T2) asks whether the respective circuit sections 411 and 412 are equivalent both topologically and geometrically) ([0099]- [0100]); and

reporting said comparison result (If two or more partitions or modules are both topologically (graph-wise) equivalent and their respective components are geometrically and/or other attribute-wise equivalent, the partitions or modules may be said to be `isomorphic`. If either the geometry/other instantiated, performance-affecting parameters or the interconnect topologies (graphs) of the two compared modules/partitions differ substantially, then the compared modules/partitions may be deemed to be `anisomorphic`; As is indicated in test step 405, if the results are true (affirmative) for each of the first through fourth tests (401-404), then the respective output signals at terminals 417 and 418 may be deemed to be substantially equivalent. In this case, a logical redundancy lock may be established for the behaviors that are to

be predicted to be found at output terminals 417 and 418. By way of example, the observed output behaviors of interest may be the magnitudes of output currents I.sub.out1 and I.sub.out2 at specific time points (e.g., t1, t2, t3, etc.) in response to respective input signals Vin1 (415) and Vin2 (416) ([0101]; [0104]- [0105]);

(10) A method comprising ([0066]- [0067]):

obtaining a first subcircuit layout design ([0119]- [0120]);

obtaining a second subcircuit layout design ([0119]- [0120]);

generating a first topology graph for said first subcircuit layout design ([0119]);

generating a second topology graph for said second subcircuit layout design ([0119]);

comparing said first topology graph and said second topology graph to obtain a comparison result ([0099]- [0100]); and

reporting said comparison result ([0101]; [0104]- [0105]);

(19) An apparatus comprising at least one processor and at least one machine-accessible medium coupled to said at least one processor, said at least one processor adapted to perform operations comprising a method of ([0066]- [0067]):

obtaining a first subcircuit layout design ([0119]- [0120]);

obtaining a second subcircuit layout design ([0119]- [0120]);

generating a first topology graph for said first subcircuit layout design ([0119]);

generating a second topology graph for said second subcircuit layout design ([0119]);

comparing said first topology graph and said second topology graph to obtain a comparison result ([0099]- [0100]); and

reporting said comparison result ([0101]; [0104]- [0105]);

(28) An apparatus comprising:

a topology graph generator to produce a first topology graph from a first subcircuit layout design and to produce a second topology graph from a second subcircuit layout design ([0119]- [0120]);

a comparator coupled to said topology graph generator, said comparator to receive said first topology graph and said second topology graph, and comparing said first topology graph and said second topology graph to obtain a comparison result ([0099]- [0100]).

With respect to claims 1-36 McGaughy teaches the features above but lacks a method/program/apparatus comprising obtaining a first whole circuit layout design and a second whole circuit layout design.

4. As to claim 1, 10, 19, and 28 Gilbert recites:

A method used by an electronic design automation system, wherein a previous integrated circuit design version and a current integrated circuit design version are partitioned into multiple cones. Each cone is defined by a path. Selected cones of logic design are compared (Abstract).

It would have been obvious to a person of ordinary skills in the art at the time the invention was made to employ Gilbert's teaching regarding the method/program/apparatus comprising obtaining a first whole circuit layout design and a

second whole circuit layout design and use it in McGaughy's invention to properly select and compare topology graphs for different versions of the same circuit layout design by providing desirable circuit design without it's functionality violation, thereby minimizing the number of iterations and time needed to arrive at an acceptable circuit design solution.

5. As to claim 2-9, 11-18, 20-27, and 29-36 McGaughy in view of Gilbert discloses:

(2), (11), (20), (29) A program/method/apparatus, wherein topology graphs comprises a plurality of nodes and lines ([0120]);

(3), (12), (21), (30) A program/method/apparatus, wherein each topology graph node comprises a data structure identifying at least one of: a node type, a node function ([0077]; [0238]-[0240]);

(4), (13), (22), (31) A program/method/apparatus, wherein said comparing comprises determining a best matching topology graph node pair ([0257]);

(5)-(9), (14)-(18), (23)-(27), (32)-(36) A program/method/apparatus, wherein if said confidence level for said topology graph node pair exceeds said best confidence level, setting a best matching topology graph node pair to said matching topology graph node pair and setting said best confidence level to said confidence level ([0027]; [0193]-[0257]).

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B. Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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THUAN DO
Primary examiner.
04/21/2006